MCM Design Using CADENCE

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Abstract - **A process of MCM design, realized by using a package of modules for the design - CADENCE, is developed. A new technology file is created on the base of data from the manufacturer and real parameters of the technological process are included. The creation of libraries and components is described. This creation is achieved through a scheme to demonstrate consistency in the design of new multi-chip module based on thin-film technology. Designed elements are described using programming language ROD. The possibilities for use of automated wiring system and possible restrictions, that can be set in the realization, are demonstrated. The checks which can detect errors occurring in the design and their elimination are shown. The functionality of the using modules of environment for design – CADENCE is described. The entire process of creating a multi-chip module is realized in ECAD laboratory at TU-Sofia.**

Keywords – Design **MCM, CADENCE, Technology file**

I. INTRODUCTION

There are many advantages of MCM, which applied them as a reasonable for use. They are: technology integration; better use of the area; large MCM can be divided into a number of schemes; information exchange and coordination of signals; simplify the design of substrate; good reliability; standardization; reasonable price. MCM structure is shown on fig.1:

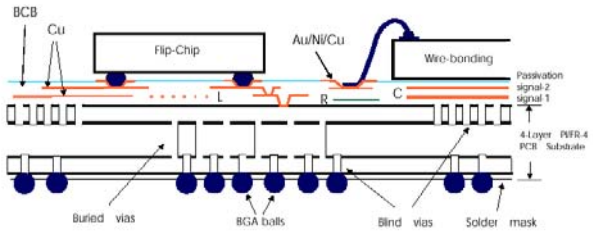

Fig. 1 MCM structure

The design is first and essential step in creation of MCM. In its basic level is determined to achieve the objective. Design should begin with a detailed specification which includes features, environment, mechanical specifications, separation of functions of conventional electrical circuits, as should be added and a strategy for testing. It's very difficult to determine the price for the design and manufacture of MCM, the price should be done before a detailed specification and to complete the distribution components. Should take into account the possibility of testing at an early stage of design. Functional test can be simplified if it is used for internal test. The design is electrical and physical. In electrical design creates netlist of modules that can be high-level description or a traditional way of an information module specification and presentation of digital /time/ analog simulation. In the physical level netlist is transformed into a layout. After the selection of substrate and placement of components on it can be done testing the system using internal testing. Components that do not work may be replaced before finally packaging and sealing.

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II. BASIC TYPES MCM

On the base substrate are formed a separate isolators and signal levels positioned one over another, in general multilayer package. The relationship between separated signal and supply levels are achieved by vias in the isolation layers. In the volume of the structure may be grounded planes or networks to improve the electromagnetic shielding of the module. On the base substrate is usually bilateral available circuits of direct current supply and input-output contact areas of the module for connection to the surrounding periphery, which may be another module, board, etc. Chips are placed on the surface of the upper isolation layer and are related to surface contact areas by bonded wire or solder balls (BGA balls) using the turn flip-chip assembly. Bonded wire is used when the input-output areas of the chips are on their perimeter and solder balls are suitable for matrix type (BGA) available on areas. Chip-resistors and chip-capacitors, diodes, transistors and IC are also mounted on the top level module. Obtained closed multi-layer structure - package may be placed in the general housing standard peripheral or matrix pins. On fig.2 are presented some typical package MCM:

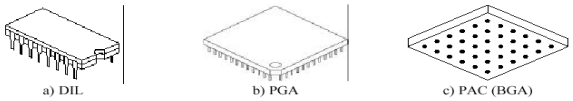

Fig. 2 Typical package MCM

MCM is divided into three groups: MCM-D; MCM-C; MCM-L. In MCM-D shown on fig.3 is used thin-film materials precipitated as a dielectric or conducting layers on the solid foundation geometric. Conducting layers consist of supply planes, signal layers and contact areas (bonding pads). Aluminum, copper, silver and gold are the materials used for conducting paths. Dielectrics are used to separate metal layers, conducting narrow or impedance paths. Can be added additional layers to realize thin-film resistors or capacitors.

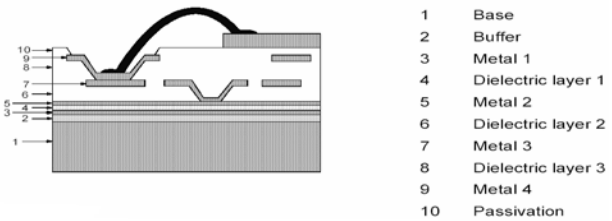

Fig. 3 MCM-D

In MCM-C, there are two general technologies:
-multiple conducting layers precipitated on ceramic substrate and located between the insolated layers.

- several conducting and ceramic layers created at high (HTCC) and the low (LTCC) temperature

All the technologies are designed for all applications: analog, digital, mixed, microwaves (with or without metal holes). Rules for design of ceramic or other basis, helping to choose appropriate technology for the application.

On fig.4 are shown two types of connections between the layers - consistent and columnar.

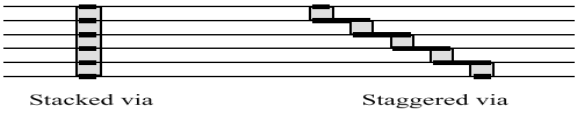

Fig. 4 Consistent and columnar connections

Contact areas and bonding in MCM-C are shown on fig.5

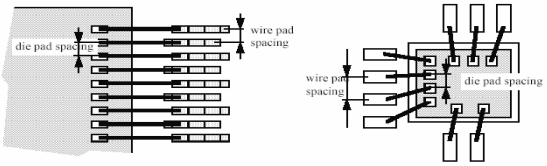

Fig. 5 Contact areas and bonding in MCM-C

Multichip module substrate with laminar MCM-L is shown on fig. 6. MCM-L technology is basically an improved PCB technology. This technology contains new or improved materials PCB - FR4, FR5, BT, etc., improved materials for solder mask-PSR 4000 and others., Surface edges for bonding - Ni / Au, Pd, SnPb, micro vias , small lines and distances between them.

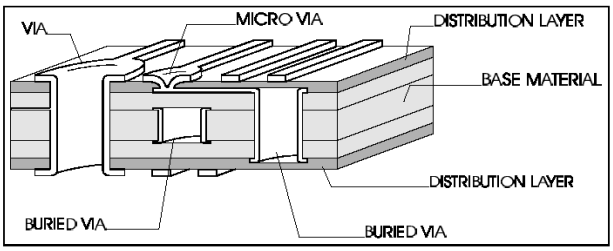

Fig. 6 MCM-L

III. Passive Components in MCM

Passive components - resistors, capacitors, coils or matrix of some of the above items, can be integrated into the MCM substrate or in discrete form on it. To choose which type of components is more appropriate to use should take into account certain parameters such as the value of the passive components, allowed substrate area, expected tolerances, etc. Layer technology is well developed in terms of resistors and occupies a major part in the production, because this technology satisfied the needs in terms of miniaturization, and allows a high density of components. Capacity and inductance, which are created in layers of hybrid substrates, occupy significant area and therefore are limited to low values. On fig.7, fig. 8 and fig. 9 are shown thin-film resistor, capacitor and coil:

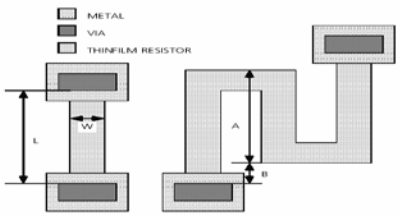

Fig. 7 Thin-film resistor

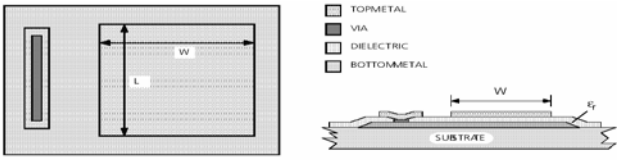

Fig. 8 Thin –film capacitor

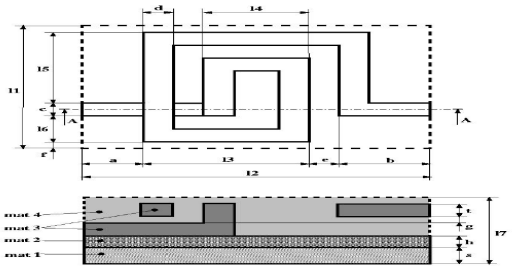

Fig. 9 Thin –film coil

Most often chips-matrices are used of R, C or RC elements which saves a lot of space

IV. Methodology and Algorithms for MCM Design Using CADENCE

Methodology for design of MCM with CADENCE is presented in block form on fig.10.

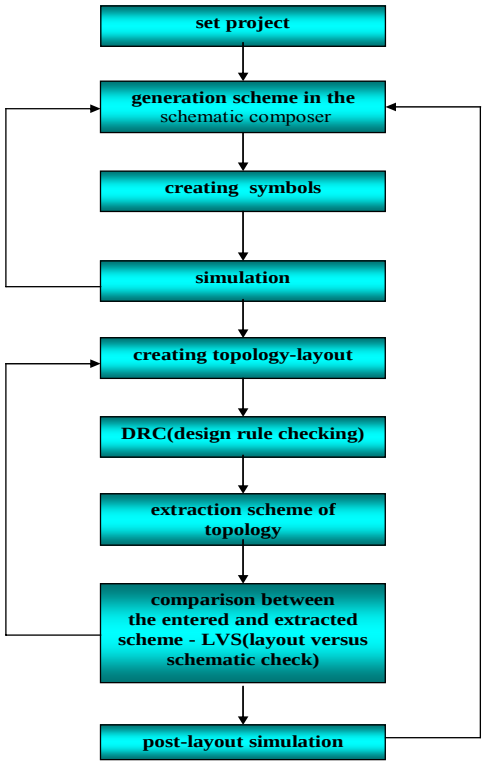

Fig. 10 Methodology for MCM design using CADENCE

Technical data in Cadence ® Design Framework II (DFII) determine the parameters used in the design. Technology information includes definitions of the layers, the definition of the elements, definition of design rules, the rules used in applications of Cadence. Technical data includes all information that sets up the structure of the project.

A. Files containing technology information and display resources

The majority of technology information is divided into two distinct types of files - technology file and display resource file. Technology file defines the rules and

materials used in the production process and contains: definitions of layers; definitions of the individual modules; electrical and physical rules. File with display resources defined the way of presentation of the layers. This file contains: definitions for the display of components; definitions of colors and lines, stylistic design; definitions of package images - it is a collection of colors and lines that are associated with a display element. Technology file associates package image to each layer.

To create a technology file is necessary to choose a particular technology, which sets the technological information needed to create multichip module. Such information for thin-film hybrid technology is provided by the MIC Technology Corporation. Below is a description of the main parameters of the technology.
-Materials used for substrate: Al_2O_3 - 99,6%; BeO; AlN.
-Materials for different layers: resistance layers -TaN - 25-150 Ω/□; NiCr - 50-250 Ω/□;
-Conducting layers - Au - 10-25 μm; Cu - 37-100 μm

The technology file contains information on the way of preparation of multichip module, description of the materials and the parameters of technological processes. This information is different for each manufacturer. When there is no such a technology file, it should be created.

On fig.11 are shown the steps of creating and using technology file on already discussed technology in environmental design Cadence Design Framework II. After creating technology file it compiles to create technology library, which contains binary technology files and presentation of the cells in it.

1. Creating ASCII technology file in language SKILL
2. Compiling technology ASCII file
3. Check for file compatibility with the technology file with requirements of individual applications
4. Attachment of the technology library to library design, cell or presentation
5. Starting session DFII for design

Fig. 11 Creating and using technology file

Technology file is organized into classes and subclasses that may be classified as sections. Class is category, in which data are grouped with similar functions. Each class begins with a name that define it: LayerRules; physicalRules; SpacingRules; electricalRules. Classes of rules for different applications define the rules that apply to specific applications related to layout in DFII (Virtuoso layout editor, layout accelerator, layout synthesizer and compactor) and applications for placement and routing. Created a technology library is attached to the design library, to cell of design library or a presentation box (cellview).

File with display resources contain information on how to display the elements, of package images of which determines how layers are displayed on the monitor, what colors and what boundary lines (fig.12). Display resource file is created with commands from the programming language SKILL.

Fig. 12 Display resources

B. Project with CADENCE DESIGN FRAMEWORK II

A library project is created. The purpose of this library is to store the project and the individual cells that can be used later in other projects without the need to design again. A new design library is presented in fig. 13

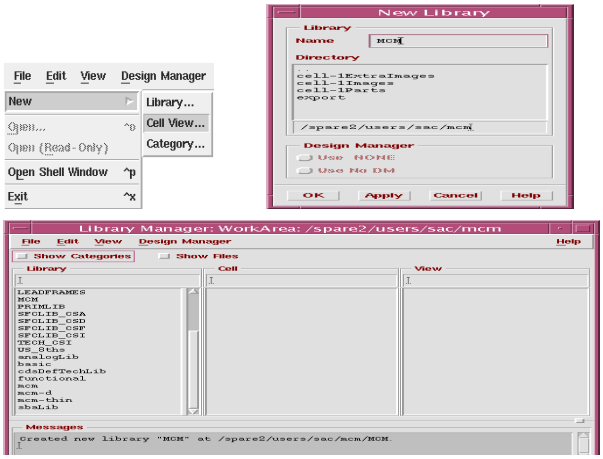

Fig. 13 Creating a library project

Elements are program designed by the language ROD (Relative Object Design). ROD is a language of high level in Cadence, which is recommended to create elements in the topology and parametric cells. It can create complex parametric element or cell. Unlike in SKILL ROD has finished functions for drawing the fundamental geometries in the topology.

V. MCM Topology Design

High-Frequency amplifier (fig. 14) is realized as multichip module. Scheme amplifier contains two high precision amplifier, which have a wide temperature range. Electric scheme has one input, one output, two supply voltages. Operational amplifiers are LM108 and LM118.

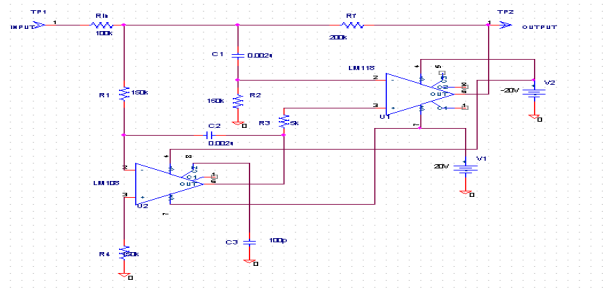

Fig. 14 High-Frequency amplifier

The scheme is implemented on the base of thin-film technology that was created in the technology file. As substrate is used Al_2O_3 99,6% in size ~ 50.8 x 50,8 mm. Resistors are designed, so for resistance material is used TaN. The terminal of the resistors were made by metallization system TiW - Ni - Au. Capacitors are

designed, as for the lower electrode is used system Cr - Cu - Au. Chromium is used as adhesives layer, copper is a electrode, which is pasivated with gold. The upper electrode is made of TiW - Ni - Au. As a dielectric between two electrodes is used polyimide for two of capacitors, and the third - silicon nitride. Contact areas for bonding and scheme pins are made from TiW - Ni - Au. Passive components are described with programming language ROD. Their parameters are given in table 1. and displayed in the working field of fig.15

TABLE 2. PASSIVE COMPONENTS PARAMETERS

comp	value, accuracy, power, current	shape and size
Rin	100K,10%, 352uW,59uA	meander - width b: 510µm distance between the shapes S: 500 µm; length l: 58,2 mm
Rf	200K,10%, 704uW,59uA	meander - width b: 505µm distance between the shapes S: 500 µm length l: 79,4 mm
R1	150K,10%, 1,6nW,1,64nA	meander - width b: 507µm distance between the S forms: 500µm; length l: 63,7 mm
R2	150K,10%, 1,6nW,104nA	meander - width b: 507 µm distance between the shapes S: 500 µm; length l: 63,7 mm
R3	5K,10%,75pW, 135nA	meander - width b: 502 µm distance between the S forms: 500µm; length l: 29,3 mm
R4	150k,10%, 1,6nW,1,6nA	meander - width b: 502 µm distance between the S forms: 500µm; length l: 29,3 mm
C1	0,002uF	area of overlap: 2.3
C2	0,002uF	area of overlap: 2.3
C3	100pF	area of overlap: 1.9

Initially are set boundaries, which will locate the components and restrict routing. In the left upper corner (in Virtuoso Layout window) is situated the input to the scheme, in the upper right corner - the output of the scheme and at the bottom are two inputs to the supply source (fig.15).

Fig.15

Areas for bonding of the two chips are situated initially around them to have enough space for situating of the components. Rectangle defines the boundaries in routing. In these boundaries are situated components and are set connections between them. In situating elements are observed several rules that facilitate subsequent routing. The most important rules are: the distances between elements to be greater of the minimum for the technology, connections between elements are possible shorter, to a small number of crossings between them, components should be placed so that the dissipated power is evenly distributed throughout the surface. Automatic routing in CADANCE can be done in a separate module - Virtuoso Chip Assembly Router. For this purpose it is necessary first to define the file of the language SKILL, which is set the way for automated routing. Routing is set to be made of two layers. To facilitate routing, paths of the two layers are in perpendicular directions, Au is in the horizontal direction and Au_2 in the vertical direction. On fig.15 is shown second window, which is used for management of the active layers. When an element or signal path out of boundaries markers are visible.

In process of designing it is necessary to set different limits. After entering all the rules and limits, can be move to routing - fig.16.

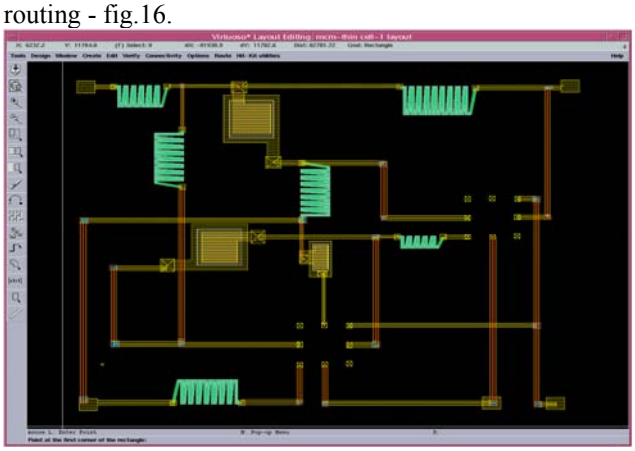

Fig.16.

Verification (Design Rule Check) serves to verify the layout, check the rules set out in the design.

II. CONCLUSION

Original resolve for design of the MCM based on the use of CADENCE was presented in this paper. Technology file was created as a already developed thin-film technology of a American company MIC technology, was described in detail its structure and manner of its creation. A new technology library was created, on its base can be designed layout. It was generated file with display resources in which were defined package images for each layer-purpose pair. File was created in programming language for object programming-ROD, in which were described the passive elements of the chosen scheme. With the realization of a particular multichip module were demonstrated qualities and benefits of the application on a developed method of design.

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